REMARKS

This Amendment is being filed in response to the Office Action mailed August 25, 2009, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1-2, 5-7 and 21 are pending in this application, where claim 1 is independent.

In the Office Action, claims 1-2, 5-7 and 21 are rejected under 35 U.S.C. §112, second paragraph. Without agreeing with the position forwarded in the Office Action and in the interest of advancing prosecution, claim 1 has been amended for better clarity and claims 4 and 10 have been canceled without prejudice. It is respectfully submitted that the rejection of 1-2, 5-7 and 21 under 35 U.S.C. §112, second paragraph has been overcome and an indication as such is respectfully requested.

In the Office Action, claims 1-2, 5-7 and 21 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,607,135 (Hirai) in view of U.S. Patent No. 6,925,008 (Ichige). Applicant respectfully

traverses and submits that claims 1-2, 5-7 and 21, as amended, are patentable over Hirai and Ichige for at least the following reasons.

Hirai is directed to IC-card module (A) that includes an IC chip 2 mounted on a substrate 1, an antenna coil 3 formed on the substrate 1, and a protective member bonded to the substrate 1 to cover the IC chip 2. As shown on FIG 1, a clearance (S) is provided between the protective member 4 and the IC chip 2 for avoiding direct contact of the protective member 4 with the IC chip 2. The clearance (S) is loaded with a filler 6 having a low modulus of elasticity, as required. The protective member 4 includes a reinforcing member 8.

Ichige is directed to a non-volatile semiconductor memory device with a memory unit including not more than two memory cell transistors. As shown in FIG 5A, selection transistors STS, STD and memory cell transistors MT1, MT2 are formed **on** a substrate 1, where the gate layers 7, 9 of the transistors STS, STD, MT1, MT2 are **covered with a mask** member insulating films 18. That is, the transistors and the mask are on the **same side** of the substrate.

It is respectfully submitted that Hirai, Ichige, and

combination thereof, do not disclose or suggest the present invention as recited in independent claim 1, which, amongst other patentable elements, recites (illustrative emphasis provided):

> an integrated circuit provided with a plurality of semiconductor elements located at the active area of the semiconductor substrate at the first surface of the semiconductor substrate, ...
>
> a mask formed **over the second surface** of the semiconductor substrate, ...
>
> wherein the mask is substantially confined at the active area over the integrated circuit and protects the integrated circuit during removal of potions of the semiconductor layer which are not covered by the mask so that the semiconductor substrate is substantially present in an area including **outside of the integrated circuit and adjacent** to the integrated circuit, and the semiconductor substrate is absent in areas between the antenna and the integrated circuit.

Hirai does not even disclose or suggest a substrate which is substantially present in an area including **outside** of the integrated circuit and **adjacent** to the integrated circuit, where the semiconductor substrate is absent in areas between the antenna and the integrated circuit. Rather, the substrate 1 shown in FIG 2 of Hirai extends along both the antenna 3 and the IC chip 2, including between the antenna 3 and the IC chip 2.

Further, any substrate within the IC chip 2, does NOT extend to areas outside the chip 2. That is, the substrate within the IC

chip 2 does NOT extend "outside of the integrated circuit and adjacent to the integrated circuit." By contrast, claim 1 recites that the substrate is included in an area "outside of the integrated circuit and adjacent to the integrated circuit and ... is absent in areas between the antenna and the integrated circuit."

Even assuming, arguendo, that somehow Hirai discloses or suggests that the substrate is included in an area "outside of the integrated circuit and adjacent to the integrated circuit and ... is absent in areas between the antenna and the integrated circuit," as recited in independent claim 1, Hirai still does not disclose or suggest any mask formed over the second surface of the semiconductor substrate, which is opposite the first surface of the semiconductor substrate that includes the integrated circuit, as correctly noted by the Examiner in the paragraph spanning pages 3-4 of the Office Action. Ichige is cited in an attempt to remedy the deficiencies in Hirai.

In Ichige, as clearly shown in FIG 5A, the transistors STS, STD, MT1, MT2 and the mask member insulating film 18 are on the **same side** of the substrate. In stark contrast, independent claim 1 recites that the "integrated circuit provided with a plurality of

semiconductor elements [are] located ... **at the first surface** of the semiconductor substrate," and the "mask [is] formed over the **second surface** of the semiconductor substrate," "the first surface being **opposite** the second surface." (Illustrative emphasis provided)

A mask formed over the second surface of the semiconductor substrate, where the second surface is **opposite** the first surface that includes the integrated circuit, as recited in independent claim 1, is nowhere disclosed or suggested in Hirai and Ichige, alone or in combination.

Accordingly, it is respectfully submitted that independent claim 1, should be allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 2, 5-7 and 21 should also be allowed at least based on their dependence from amended independent claim 1.

In addition, Applicant denies any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicant reserves the right to

submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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